AMD Opteron™ processors scalability and Roadmap

HPC Advisory Council Switzerland Workshop 2010
Dr. Ing. Hervé Chevanne | March 17, 2010
AMD’s HPC Product Portfolio

Energy efficient CPU and discrete GPU processors focused on addressing the most demanding HPC workloads

**Multi-core x86 Processors**
- Outstanding Performance
- Superior Scalability
- Enhanced Power Efficiency

**Professional Graphics**
- 3D Accelerators For Visualization
- See More and Do More with Your Data

**ATI Stream Computing**
- GPU Optimized For Computation
- Massive Data-parallel Processing
- High Performance Per Watt
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### Planned Server Platform Roadmap

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<thead>
<tr>
<th>Year</th>
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</tr>
</thead>
<tbody>
<tr>
<td>2/4-way Enterprise Platform</td>
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<td>“Maranello”</td>
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<td>Socket F(1207) with AMD SR56x0 and SP5100</td>
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<td>&quot;Shanghai&quot;/&quot;Istanbul&quot;</td>
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<tr>
<td>1/2-way Power Efficient Platform</td>
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<td>“Socket F (1207)”</td>
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<tr>
<td>1-way Platform</td>
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<td>“San Marino”</td>
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<td>Socket C32+AMD SR56x0 and SP5100</td>
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<td></td>
<td>“Lisbon” New Architecture</td>
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<td>“Adelaide”</td>
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<td></td>
<td>Socket C32 EE+AMD SR5650 and SP5100</td>
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<td>“Lisbon” New Architecture</td>
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<td></td>
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<td></td>
<td>“Buenos Aires”</td>
<td></td>
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<td></td>
<td>Socket AM3 with AMD SR56x0 and SP5100</td>
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<td></td>
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<td></td>
<td></td>
<td></td>
<td>&quot;Suzuka&quot;</td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td>“Socket AM2+”</td>
<td></td>
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<td></td>
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<td></td>
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<td></td>
</tr>
</tbody>
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</tr>
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<tr>
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Server/WS Chipset Roadmap

Mainstream

RD790*
- HT3
- PCI-E Gen2
- 38 lanes
- 1S only

S: Now
P: Now

SR5690
- HT3
- PCI-E Gen2
- 42 lanes
- IOMMU
- RAS features
- Up to 8S support

P: Now

SR5670
- HT3
- PCI-E Gen2
- 30 lanes
- IOMMU
- RAS features
- Up to 2S support

P: Now

SR5650
- HT3
- PCI-E Gen2
- 22 lanes
- IOMMU
- 1S only

P: Now

Entry

RS780*
- HT3
- PCI-E Gen2
- 22 lanes
- Integrated Graphics
- 1S only

S: Now
P: Now

Server/WS Chipset

SB700*
- 6 SATA 3Gb/Sec
- 12+2 USB Ports
- PCI 2.3

S: Now
P: Now

SR5700
- HT3
- PCI-E Gen2
- 30 lanes
- IOMMU
- RAS features
- Up to 2S support

P: Now

SR5500
- HT3
- PCI-E Gen2
- 22 lanes
- IOMMU
- 1S only

P: Now

2008

2009

SB

SP5100
- 6 SATA 3Gb/Sec
- 12+2 USB Ports
- PCI 2.3

P: Now

*Workstation only
# x86 64-bit Architecture Evolution

<table>
<thead>
<tr>
<th>Year</th>
<th>Mfg. Process</th>
<th>CPU Core</th>
<th>L2/L3</th>
<th>Hyper Transport™ Technology</th>
<th>Memory</th>
</tr>
</thead>
<tbody>
<tr>
<td>2003</td>
<td>90nm SOI</td>
<td>K8</td>
<td>1MB/0</td>
<td>3x 1.6GT/.s</td>
<td>2x DDR1 300</td>
</tr>
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<td>2005</td>
<td>90nm SOI</td>
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</tr>
<tr>
<td>2007</td>
<td>65nm SOI</td>
<td>“Greyhound”</td>
<td>512kB/2MB</td>
<td>3x 2GT/s</td>
<td>2x DDR2 667</td>
</tr>
<tr>
<td>2008</td>
<td>45nm SOI</td>
<td>“Greyhound+”</td>
<td>512kB/6MB</td>
<td>3x 4.0GT/s</td>
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</tr>
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Power Efficient Innovations

**AMD Smart Fetch Technology**
Can reduce power consumption by allowing idle cores to enter a "halt" state.

**AMD PowerCap Manager**
Allows IT datacenter managers to set a fixed limit on a server's processor power consumption.

**Dual Dynamic Power Management**
Enables more granular power management capabilities to reduce processor energy consumption. Separate power planes for cores and memory controller.

**AMD PowerNow!™ Technology with Independent Dynamic Core Technology**
Allows processors and cores to dynamically operate at lower power and frequencies, depending on usage and workload to help reduce TCO and to lower power consumption in the datacenter.

**Enhanced Performance-per-watt**
50% more compute cores vs. quad-core within the same power envelope.*

**AMD CoolCore™ Technology**
Can reduce processor energy consumption by dynamically turning off sections of the processor when inactive. Extends to the L3 Cache.

**HyperTransport™ technology**
Links provide up to 57.6 GB/s of Bandwidth per processor.

**12.8 GB/s DDR2-800**

*Compared to Quad-Core AMD Opteron processor codenamed "Shanghai."
Six-Core AMD Opteron™ Processor

- Six true cores
- New HyperTransport™ technology HT Assist
- Increased HyperTransport™ 3 technology (HT3) bandwidth
- Higher performing Integrated Memory Controller
- Same power/thermal ranges as Quad-Core AMD Opteron™ processor
- Up to 50% higher performance than Quad-Core AMD Opteron™ processor-based servers at the same processor ACP *

(*) Based on SPECint® 2006 results published as of 11/09/09. See backup slides for configuration and performance information.
Six-Core AMD Opteron™ Processor

Performance
- Six-Core AMD Opteron™ Processor
  6M Shared L3 Cache
  North Bridge enhancements (PF + prefetch)
  45nm Process Technology
- DDR2-800 Memory
- HyperTransport™ 3 technology @ up to 4.8 GT/sec

Reliability/Availability
- L3 Cache Index Disable
- HyperTransport Retry (HT-3 Mode)
- x8 ECC (Supports x4 Chipkill in unganged mode)

Virtualization
- AMD Virtualization™ (AMD-V™) technology with Rapid Virtualization Indexing

Manageability
- APML Management Link*

Scalability
- 48-bit Physical Addressing (256TB)
- HT Assist (Cache Probe Filter)

Continued Platform Compatibility
- Nvidia/Broadcom-based F/1207 platforms

(*) APML-enabled platform support required.

SE: 2.8GHz
Std: 2.6GHz
HE: 2.1GHz
EE: 1.8GHz
The Memory Bandwidth

Memory Bandwidth: is the rate at which data can be read from or stored into a semiconductor memory by a processor

Memory Bandwidth at the DIMM level

= 64bits x 0.8GHz x 2ch.
= 12.8GB/s per processor
Six-Core AMD
Opteron™ Processor

Performance
• Six-Core AMD Opteron™ Processor
  6M Shared L3 Cache
  North Bridge enhancements (PF + prefetch)
  45nm Process Technology
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• 48-bit Physical Addressing (256TB)
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Continued Platform Compatibility
• Nvidia/Broadcom-based F/1207 platforms

STREAM Bandwidth (GB/s)*

<table>
<thead>
<tr>
<th>Product, Freq, Dram</th>
<th>2S</th>
<th>4S</th>
<th>8S</th>
</tr>
</thead>
<tbody>
<tr>
<td>“Barcelona,” 2.3/2.0, RDDR2-667</td>
<td>17.2</td>
<td>20.5</td>
<td></td>
</tr>
<tr>
<td>“Shanghai,” 2.7/2.2, RDDR2-800</td>
<td>21.4</td>
<td>24</td>
<td></td>
</tr>
<tr>
<td>“Istanbul,” 2.4/2.2, RDDR2-800</td>
<td>22</td>
<td>42</td>
<td>81.5</td>
</tr>
</tbody>
</table>

(*) Based on measurements at AMD performance labs. See backup slide for configuration information.
A simple Kernel Analysis

- STREAM Triad:
  \[ A[i] = B[i] + q \times C[i] \]
- Each iteration:
  - requires load of 2x64 bits words \((B[i] \text{ and } C[i])\) and stores 1x64 bits word \((A[i])\)
  - performs 2x64bits floating point operations
    \((1 \text{ ADD and } 1 \text{ MUL})\)

\[ \Rightarrow \text{Achieving 2 FP operations requires 2 LOAD and 1 STORE} \]

**Computational Intensity:** \((2 \text{ FPops} / 3 \text{ LDST}) = 0.67\)
Another example: Coupled Maxwell Equations

\[\begin{align*}
\text{DO } K &= 2, \text{NZ}-1; \text{ DO } J = 2, \text{NY}-1; \text{ DO } I = 2, \text{NX}-1 \\
HX(I,J,K) &= C11EDX(I,J,K) \ast (HX(I,J,K) - (EZ(I,J,K) \ast C12HDY(I,J,K) - C12HDY(I,J-1,K) \ast EZ(I,J-1,K)) + (EY(I,J,K) \ast C12HDZ(I,J,K) - C12HDZ(I,J,K-1) \ast EX(I,J,K-1))) \\
HY(I,J,K) &= C11EDY(I,J,K) \ast (HY(I,J,K) - (EX(I,J,K) \ast C12HDZ(I,J,K) - C12HDZ(I,J,K-1) \ast EX(I,J,K-1)) + (EZ(I,J,K) \ast C12HDX(I,J,K) - C12HDX(I-1,J,K) \ast EZ(I-1,J,K))) \\
HZ(I,J,K) &= C11EDZ(I,J,K) \ast (HZ(I,J,K) - (EY(I,J,K) \ast C12HDX(I,J,K) - C12HDX(I-1,J,K) \ast EY(I-1,J,K)) + (EX(I,J,K) \ast C12HDY(I,J,K) - C12HDY(I-1,J,K) \ast EX(I-1,J,K))) \\
EX(I,J,K) &= C22HDX(I,J,K) \ast (EX(I,J,K) - (HZ(I,J,K) \ast C21EDY(I,J,K) - C21EDY(I,J-1,K) \ast HZ(I,J-1,K)) + (HY(I,J,K) \ast C21EDZ(I,J,K) - C21EDZ(I,J,K-1) \ast HY(I,J,K-1))) \\
EY(I,J,K) &= C22HDY(I,J,K) \ast (EY(I,J,K) - (HX(I,J,K) \ast C21EDZ(I,J,K) - C21EDZ(I,J,K-1) \ast HX(I,J,K-1)) + (HZ(I,J,K) \ast C21HDX(I,J,K) - C21HDX(I-1,J,K) \ast HZ(I-1,J,K))) \\
EZ(I,J,K) &= C22HDZ(I,J,K) \ast (EZ(I,J,K) - (HY(I,J,K) \ast C21HDX(I,J,K) - C21HDX(I-1,J,K) \ast HY(I-1,J,K)) + (HX(I,J,K) \ast C21HDY(I,J,K) - C21HDY(I-1,J,K) \ast HX(I,J-1,K)))
\end{align*}\]

ENDDO; ENDDO; ENDDO

66 LOADS/STORES for 54 FP operations

Computational Intensity: \((54 \text{ FOps} / 66 \text{ LDST}) = 0.82\)
FP Intensive vs. Memory Intensive
## x86 64-bit Architecture Evolution

<table>
<thead>
<tr>
<th>Year</th>
<th>Mfg. Process</th>
<th>CPU Core</th>
<th>X87</th>
<th>SSE</th>
<th>SSE2</th>
</tr>
</thead>
<tbody>
<tr>
<td>2003</td>
<td>90nm SOI</td>
<td>K8</td>
<td></td>
<td>(2 Mul + 2 Add)/cycle (32bits)</td>
<td>(1 Mul + 1 Add)/cycle (64bits)</td>
</tr>
<tr>
<td>2005</td>
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<td></td>
<td>(4 Mul + 4 Add)/cycle (32bits)</td>
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Parallel Scalability of Real Applications
VASP 4.6 Test configuration

AMD DMZ server configuration:

- Tyan S4987 (4 Sockets)
  - 4xOpteron™ 8435 (2.6GHz/2.2GHz)
  - 8x(4GB+2GB) DDR2-667 registered
- SLES 10.1 vanilla
- VASP 4.6
- FFTW 3.2
- PGI 8.0-6
- OPENMPI 1.3.2 with NUMA placement ("numactl")
VASP 4.6
(http://cms.mpi.univie.ac.at/vasp)

Paracetamol – 8 molecules
Parallel Speed-Up
(Higher values are better)
HIRLAM 7.0 Test Configuration

AMD DMZ server configuration:
- AMD “toonie” reference design (2 Sockets)
  2xOpteron™ 2435 (2.6GHz/2.2GHz)
  8x4GB DDR2-800 registered (32GB in total)
- SLES 11
- OPEN64 4.2.2.9
- OPENMPI 1.3.3 with NUMA placement ("numactl")
The HIRLAM System was developed by the HIRLAM Programme group, a co-operative Programme of the national weather services in Denmark, Finland, Iceland, Ireland, the Netherlands, Norway, Spain and Sweden.
GADGET-2 2.0.4 Test Configuration

AMD DMZ server configuration:
- AMD “toonie” reference design (2 Sockets)
  2xOpteron™ 2435 (2.6GHz/2.2GHz)
  8x4GB DDR2-800 registered (32GB in total)
- SLES 11
- OPEN64 4.2.3
- OPENMPI 1.4.1 with NUMA placement ("numactl")
GADGET-2 2.0.4
(http://www.mpa-garching.mpg.de/gadget)

(*) Cosmological formation of a cluster of galaxies (collisionless, vacuum boundaries)
2010 Server Roadmap
## x86 64-bit Architecture Evolution

<table>
<thead>
<tr>
<th></th>
<th>2003</th>
<th>2005</th>
<th>2007</th>
<th>2008</th>
<th>2009</th>
<th>2010*</th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>Mfg. Process</strong></td>
<td>AMD Opteron™</td>
<td>AMD Opteron™</td>
<td>“Barcelona”</td>
<td>“Shanghai”</td>
<td>“Istanbul”</td>
<td>“Magny-Cours”</td>
</tr>
<tr>
<td></td>
<td>90nm SOI</td>
<td>90nm SOI</td>
<td>65nm SOI</td>
<td>45nm SOI</td>
<td>45nm SOI</td>
<td>45nm SOI</td>
</tr>
<tr>
<td><strong>CPU Core</strong></td>
<td>K8</td>
<td>K8</td>
<td>“Greyhound”</td>
<td>“Greyhound+”</td>
<td>“Greyhound+”</td>
<td>“Greyhound+”</td>
</tr>
<tr>
<td></td>
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<td></td>
<td></td>
<td></td>
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</tr>
<tr>
<td><strong>L2/L3</strong></td>
<td>1MB/0</td>
<td>1MB/0</td>
<td>512kB/2MB</td>
<td>512kB/6MB</td>
<td>512kB/6MB</td>
<td>512kB/12MB</td>
</tr>
<tr>
<td><strong>Hyper Transport™ Technology</strong></td>
<td>3x 1.6GT/s</td>
<td>3x 1.6GT/s</td>
<td>3x 2GT/s</td>
<td>3x 4.0GT/s</td>
<td>3x 4.8GT/s</td>
<td>4x 6.4GT/s</td>
</tr>
<tr>
<td><strong>Memory</strong></td>
<td>2x DDR1 300</td>
<td>2x DDR1 400</td>
<td>2x DDR2 667</td>
<td>2x DDR2 800</td>
<td>2x DDR2 800</td>
<td>4x DDR3 1333</td>
</tr>
</tbody>
</table>

(*) Planned model or feature introduction dates.
Server Roadmap

**4-way Performance Platform**
- **“Shanghai” 4-Core**
  - 6M L3
  - 3x HT-3 (4.4GT)
  - AMD-V technology
  - DDR2 (Dual-Channel)

- **“Istanbul” 6-Core**
  - 8M L3
  - 3x HT-3 (4.8GT)
  - HT Assist
  - AMD-V technology
  - DDR2 (Dual-Channel)

**2 and 4-way Enterprise/Mainstream Platform**
- **“Magny-Cours” 8/12-Core**
  - 12M L3
  - 4x HT-3 (6.4GT)
  - U/RDDR3 & LV RDDR3 (Quad-Channel)
  - Cool Speed
  - C1E
  - AMD-V
  - HT Assist

**2-way Mainstream Platform**
- **“Maranello”**
  - Maximum Scalability
  - AMD SR56x0
  - AMD SP5100
  - Advanced Platform Management

**1-way Mainstream Platform**
- **“Budapest” 4-Core**
  - 6M L3
  - DDR3
  - 1xHT3
  - AMD-V technology

- **“Suzuka” 4-Core**
  - 6M L3
  - DDR3
  - AMD-V technology

**1 and 2-way Energy Efficient/Cost Optimized Platform**
- **“San Marino” (Std/HE/EE)**
  - Optimized Energy Efficiency
  - AMD SR56x0
  - AMD SP5100
  - Advanced Platform Management

- **“Buenos Aires”**
  - AMD SR56x0
  - AMD SP5100

**Ultra Low Power**
- **“Adelaide” (EE Only)**
  - Ultra Low Power
  - AMD SR5650
  - AMD SP5100
  - LV DDR3
  - HT1

(*) Planned model or feature introduction dates
AMD 2010-2011 Sweet Spot Server Strategy

Performance-per-watt and Expandability

- 4P/8P Platforms (~5% of Market*)
- 2P Platforms (~75% of Market*)
- 1P Platforms (~20% of Market*)

Platform Consistency and Commonality

- AMD Opteron™ 6000 Series Platform
  “Magno-Cours” 8 and 12 cores
  “Interlagos” 12 and 16 cores
  - 2/4 socket; 4 memory channels
  - Highly scalable without compromising value

Highly Energy Efficient and Cost Optimized

- AMD Opteron™ 4000 Series Platform
  “Lisbon” 4 and 6 cores
  “Valencia” 6 and 8 cores
  - 1/2 socket; 2 memory channels
  - New levels of value and power efficiency

(*) AMD internal estimates of total server market as of Q309
(**) Planned model or feature introduction dates
The AMD Opteron™ 6100 Series Processor

- **Target:** Enterprise Class 2-way and 4-way Servers
  - Twelve-core and Eight-core 12M L3 Cache
  - AMD CoolCore™ technology, Enhanced AMD PowerNow!™ technology, Enhanced C1 state, CoolSpeed technology, APML*
  - Quad-Channel LV & U/RDDR3, ECC, On-line spare memory support
  - Up to 3 DIMMs/channel, 12 per CPU
  - Expected platforms 2P/2U, 2P Tower, 4P rack, 4P Blade

- **Single Series** for performance DP and MP platforms
  - 2P economics for 4P servers
  - Compelling price/performance for volume market

- **G34 Socket Infrastructure**
  - Performance-optimized Power/thermals
  - Quad 16-bit HT3 links, up to 6.4 GT/s per link
  - AMD SR56x0 chipset with AMD-Vi and PCIe® Gen2

(*) In APML-enabled systems
AMD Opteron™ 6100 Series Processor Logical View and Example Topologies

2P

Diameter 1
Avg Diam 0.75
DRAM BW 85.3 GB/s
XFIRE BW 71.7 GB/s

4P

Diameter 2
Avg Diam 1.25
DRAM BW 170.6 GB/s
XFIRE BW 143.4 GB/s

16bits
8bits
16bits
16bits
DDR3
HyperTransport™ 3 technology
AMD Opteron™ 6100 Series Processor Memory Bandwidth

“Magny-Cours” vs. “Istanbul”:
Up to x3.3 memory bandwidth per proc.
Up to x2.0 core count per proc.

Memory Bandwidth at the DIMM level
= 64bits x 1.333GHz x 4ch.
= 42.6GB/s per processor
2011 Server Roadmap
**Server Roadmap**

1. **4-way Performance Platform**
   - **“Shanghai”**
     - 4-Core
     - 6M L3
     - 3x HT-3 (4.4GT)
     - AMD-V technology
     - RDOR2 (Dual-Channel)
   - **“Istanbul”**
     - 6-Core
     - 6M L3
     - 3x HT-3 (4.8GT)
     - HT Assist
     - AMD-V technology
     - RDOR2 (Dual-Channel)

2. **2-way Mainstream Platform**
   - **“Socke F (1207)”**
   - **Six-Core AMD Opteron™ Processor w/AMD Chipset**
     - AMD SR56x0
     - AMD SP5100

3. **1-way Platform**
   - **“Budapest”**
     - 4-Core
     - 6M L3
     - DDR3
     - 1xHT1
     - AMD-V technology
   - **“Suzuka”**
     - 4-Core
     - 6M L3
     - DDR3
     - 1xHT1
     - AMD-V technology

4. **Platform Segment**
   - **2009**
   - **2010**
   - **2011**

5. (***) Planned model or feature introduction dates

6. (Yellow text denotes new feature)
Introducing the AMD Processor Architecture Codenamed "Bulldozer"

- "Bulldozer" is an innovative new architecture that offers the potential of dramatically reducing the thread-interference.

- AMD is planning to deliver highly scalable industry-standard processor architecture with true core functionality.

- "Bulldozer" is a modular architecture that creates the building blocks of the next generation of processor designs.
The ability to execute two threads on two discrete, unshared cores without compromising or creating bottlenecks.

**“Bulldozer” module**

Two cores in a single unit that enables two simultaneous threads, the building blocks of a “Bulldozer” die.

**Parallel Threads**

The ability to execute two threads on two discrete, unshared cores without compromising or creating bottlenecks.

**Flex FP**

A flexible floating point unit that can be dedicated OR shared between the two cores per cycle.

**Dedicated Scheduler**

Independent integer schedulers and an FP scheduler improve scalability by efficient execution.
THANK YOU
BACKUP AND CONFIGURATION INFORMATION
Two-Socket SPECint®_rate2006 – Slide 10

205 using 2 x Six-Core AMD Opteron™ processors (“Istanbul”) Model 2435 in Supermicro A+ Server 1021M-UR+B server, 32GB (8x4GB DDR2-800) memory, 250GB SATA disk drive, SuSE Linux® Enterprise Server 10 SP2 64-bit

136 using 2 x Quad-Core AMD Opteron™ processors (“Shanghai”) Model 2384 in Supermicro A+ Server 1021M-UR+B server, 32GB (8x4GB DDR2-800) memory, 250GB SATA disk drive, SuSE Linux® Enterprise Server 10 SP2 64-bit

Two-Socket STREAM – Slide 13

21GB/s using 2 x Six-Core AMD Opteron™ processors (“Istanbul”) Model 2435 in Supermicro H8DMU+ motherboard, 16GB (8x2GB DDR2-800) memory, SuSE Linux® Enterprise Server 10 SP1 64-bit

21GB/s using 2 x Quad-Core AMD Opteron™ processors (“Shanghai”) Model 8384 in Supermicro H8DMU+ motherboard, 16GB (8x2GB DDR2-800) memory, SuSE Linux® Enterprise Server 10 SP1 64-bit

Four-Socket STREAM – Slide 13

42GB/s using 4 x Six-Core AMD Opteron™ processors (“Istanbul”) Model 8435 in Tyan Thunder n4250QE (S4985-E) motherboard, 32GB (16x2GB DDR2-800) memory, SuSE Linux® Enterprise Server 10 SP1 64-bit (with HT Assist enabled)

24GB/s using 4 x Quad-Core AMD Opteron™ processors (“Shanghai”) Model 8384 in Tyan Thunder n4250QE (S4985-E) motherboard, 32GB (16x2GB DDR2-800) memory, SuSE Linux® Enterprise Server 10 SP1 64-bit
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