Scientific Computing with Intel Xeon Phi Coprocessors

Andrey Vladimirov
Colfax International

HPC Advisory Council Stanford Conference 2015
Contents

§1 MIC Architecture, Developer’s Perspective

§2 Case Studies
  - Astrophysics (offload story)
  - N-body simulation (offload vs native in a cluster)
  - Financial Monte Carlo (heterogeneous clustering)
  - Computational fluid dynamics (legacy code)

§3 Colfax Developer Training
§1. MIC Architecture from Developer’s Perspective
Intel Xeon Phi Coprocessors and the MIC Architecture

- PCIe end-point device
- High Power efficiency
- ~ 1 TFLOP/s in DP
- Heterogeneous clustering

For highly parallel applications which reach the scaling limits on Intel Xeon processors
Examples of Solutions with the Intel MIC Architecture

Colfax’s CXP7450 workstation with two Intel Xeon Phi coprocessors
[link: xeonphi.com/workstations]

Colfax’s CXP9000 server with eight Intel Xeon Phi coprocessors
[link: xeonphi.com/servers]
Intel Xeon Phi Coprocessors and the MIC Architecture

- ≤18 cores/socket ≈3 GHz
- 2-way hyper-threading
- Up to 768 GB of DDR3 RAM
- 256-bit AVX vectors

- 57 to 61 cores at ≈1 GHz
- 4 hardware threads per core
- 6–16 GB cached GDDR5 RAM
- 512-bit IMCI vectors

- C/C++/Fortran; OpenMP/MPI
- Linux OS (on host and on coprocessor)
Linux µOS on Intel Xeon Phi coprocessors (part of MPSS)

```
user@host% lspci | grep -i "co-processor"
06:00.0 Co-processor: Intel Corporation Xeon Phi coprocessor 3120 series (rev 20)
82:00.0 Co-processor: Intel Corporation Xeon Phi coprocessor 3120 series (rev 20)
```

```
user@host% sudo service mpss status
mpss is running
```

```
user@host% cat /etc/hosts | grep mic
172.31.1.1 host-mic0 mic0
172.31.2.1 host-mic1 mic1
```

```
user@host% ssh mic0
user@mic0% cat /proc/cpuinfo | grep proc | tail -n 3
processor : 237
processor : 238
processor : 239
```

```
user@mic0% ls /
amplxe  dev   home  lib64  oldroot  proc  sbin  sys  usr
bin   etc   lib  linuxrc  opt  root  sep3.10  tmp  var
```
Offload and Native modes

- Explicit offload mode:
  ```c
  Host
  main() {
  #pragma offload target(mic)
  }
  Coprocessor
  myFunction();
  ```

- Native mode:
  ```c
  Host
  Coprocessor
  main() {
  myFunction();
  }
  ```
Optimization Areas

Common methods for Intel Xeon CPUs and Intel Xeon Phi coprocessors:

1. **Scalar optimization** (compiler-friendly practices)
2. **Vectorization** (must use 16- or 8-wide vectors)
3. **Multi-threading** (must scale to 100+ threads)
4. **Memory access** (streaming access or tiling)
5. **Communication** (offload, MPI traffic control)
Getting Ready for the Future

- Knights Landing (KNL) – next generation of Intel MIC architecture
- 3x the performance of current generation
- Available as a stand-alone processor or as a coprocessor
The best way to prepare applications for KNL is to optimize them for Intel Xeon Phi coprocessors based on KNC.
§2. Case Studies
Astrophysical Code HEATCODE: an Offload Story

Porting to Intel® Xeon Phi™ coprocessors
- We ported Frankie code using explicit offload model
- Same code & optimization methods for Xeon Phi™
- Simultaneous calculations on CPU and coprocessors with automatic load balancing was easy to implement
- With two Intel® Xeon Phi™ coprocessors, performance for high-res calculations is 3.2x better than with two Intel® Xeon® E5 processors alone.
- RESULT: estimated target project calculation time is now 2 weeks (down from 6+ years)

Goal achieved!

xeonphi.com/papers/heatcode
Astrophysical Code HEATCODE: an Offload Story

xonphi.com/papers/heatcode
N-body Simulation: Offload vs Native in a Cluster

Compute device: | 2 Intel Xeon CPUs | 1 Intel Xeon Phi coprocessor | 2 Intel Xeon Phi coprocessors
---|---|---|---
Problem size | N=40000 | N=40000 | N=40000
Performance | 5.98 steps per second | 23.62 steps per second | 44.21 steps per second

xeonphi.com/papers/nbody-basic
N-body Simulation: Offload vs Native in a Cluster

N-Body Simulation Performance

Processor: Intel Xeon E5-2697 v2
Coprocessor: Intel Xeon Phi 7120P

Single Precision GFLOP/s

0 500 1000 1500 2000

5.3 0.8
Initial

140 120
Multithreaded

180 220
Vectorized with SoA

480
Scalar Tuning

870

520
Tiled, Unrolled

1620

xeonphi.com/papers/sc14
N-body Simulation: Offload vs Native in a Cluster

Performance, TFLOP/s

Number of Nodes or Coprocessors (P)

Intel Xeon E5-2697 v2 CPUs (4 nodes)
Intel Xeon Phi 7120P coprocessors (4 per node)
N=2^{20} particles (strong scaling)

1 Xeon Phi/node
2 Xeon Phi/node
3 Xeon Phi/node
4 Xeon Phi/node

CPU
Xeon Phi, native MPI
Xeon Phi, MPI+Offload

xeonphi.com/papers/sc14
Asian Option Pricing: Heterogeneous Clustering

Heterogeneous Clustering with Homogeneous Code: Asian Option Pricing

Done!

Relative Performance

0 1 2 3 4
CPUs Coprocessors All

Network MPI Communication

Boss rank=0

Worker rank=1
192.168.9.10 compute-01
192.168.9.12 compute-02
192.168.9.11 compute-01-mic0
192.168.9.20 compute-02-mic0
192.168.9.21 compute-01-mic1
192.168.9.22 compute-02-mic1

Worker rank=2
Worker rank=3
Worker rank=4
Worker rank=5
Worker rank=6

xenonphi.com/papers/heterogeneous
Computational Fluid Dynamics: Legacy Code

Fluid Dynamics with Fortran on Intel® Xeon Phi™ Coprocessors

Shallow Water Equation Solver

Same code for CPU and Xeon Phi
Fortran 90 + OpenMP + MPI

Publication:
Xeonphi.com/papers/shallow

Performance on CPU: 19.5 GFLOP/s
Performance with Coprocessors: 52.5 GFLOP/s

Simulation Size: 9600x9600
Acceleration: 2.7X

Intel Xeon E5-2697 v3 Processor

Intel Xeon E5-2697 v3 Processor + Two Intel Xeon Phi 7120A Coprocessors

www.colfax-intl.com
§3. Colfax Developer Training
Colfax Developer Training

Intel Xeon Phi Coprocessor Programming
Future-Proofing Applications for Knights Landing (KNL)

xeonphi.com/training
Free Training for HPCAC Stanford 2015 Participants

COLFAX DEVELOPER TRAINING FOR INTEL® XEON PHI™ COPROCESSOR

FOR A LIMITED TIME, COLFAX INTERNATIONAL IS OFFERING FREE 1-DAY AND 4-DAY CLASSES! CLASS SEATS ARE LIMITED.
SIGN UP AT: XEONPHI.COM/HPCAC2015

CDT 101: 1-DAY LECTURE SERIES
PROGRAMMING MODELS, PARALLEL FRAMEWORKS AND OPTIMIZATION PRACTICES FOR INTEL XEON PHI COPROCESSORS. LECTURE-ONLY TRAINING. PREREQUISITE FOR CDT 102.

CDT 102: 1-DAY HANDS-ON LABS
HANDS-ON EXERCISES ON PROGRAMMING INTEL XEON PHI COPROCESSORS. TUTORIALS ON EXPRESSING PARALLELISM AND OPTIMIZING PERFORMANCE WITH A FOCUS ON METHODS APPLICABLE TO MULTI-CORE CPUs AS WELL AS INTEL MIC ARCHITECTURE. PREREQUISITE: CDT 101.

CDT 401: 4-DAY WORKSHOP
IN-DEPTH DISCUSSION AND EXERCISES ON PROGRAMMING INTEL XEON PHI COPROCESSORS, INCLUDING HETEROGENEOUS CLUSTERING WITH NATIVE AND OFFLOAD METHODS. NUMEROUS HANDS-ON EXAMPLES ON TUNING THE PERFORMANCE OF SCALAR MATH, VECTORIZATION, MULTI-THREADING, MEMORY TRAFFIC AND COMMUNICATION.

xeonphi.com/hpcac2015