CPU / GPU TECHNOLOGIES
NOW AND FUTURE

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Current trajectory puts traditional x86 computing at just over 20Pflops by 2018

A data center that could achieve an exaflop in 2018 using only x86 processors would consume over 3TW

To achieve exascale capability by 2018, x86 performance would need to increase by 2x each year, starting in 2010

Heterogeneous compute required to bridge the gap

Homogeneous x86 compute hits a wall
**HIGH EFFICIENCY LINPACK IMPLEMENTATION ON AMD MAGNY COURS + AMD 5870 GPU**

**System GFLOPS**

- **DGEMM/node**
- **Linpack/node**
- **Linpack/4 nodes**

**Graphical Representation**

- **GPU DPFP Peak:** 544 GFLOPS
- **GPU DGEMM kernel:** 87% of Peak
- **2.5 GFLOPS/W**
- **Node DPFP Peak:** 745.6 GFLOPS
- **Linpack efficiency:** 75.5% of Peak
- **Linpack scaling across 4 nodes:** 70% of Peak

**HPL code:**

[http://code.compeng.uni-frankfurt.de/](http://code.compeng.uni-frankfurt.de/)
AMD PROCESSOR POWER AND PERFORMANCE OVER TIME
INCREASING PERFORMANCE-PER-WATT EFFICIENCIES

SPEC, SPECint, and SPECfp are registered trademarks of the Standard Performance Evaluation Corporation. The comparison presented above is based on the best performing two-socket servers using the specified processor model. For the latest SPECint_rate2006 and SPECfp_rate2006 results, visit http://www.spec.org/cpu2006/results.

"Interlagos" performance based on internal AMD estimates.
Compared to how the current architecture handles two threads, “Bulldozer” can deliver more performance in a smaller die space.
The “Bulldozer” module has shared and dedicated components

The shared components:
- Help reduce power consumption
- Help reduce die space (cost)

The dedicated components:
- Help increase performance and scalability

“Bulldozer” dynamically switches between shared and dedicated components to maximize performance per watt
- Co-processor organization
- Reports completion back to parent core
- Dual 128-bit FMAC pipes
- Dual 128-bit packed integer pipes
- PRF-based register renaming
- Unified scheduler (for both threads)
Each core is logical processor from viewpoint of software

![Diagram of thread control and selection mechanisms.]

- IF thread domain
- Decode thread domain
- Dispatch thread domain
- Core
- SC Qs
- Core
- FP frontend
- FP Execution
- FP backend
- PredQ
- IBB
- uopQ
- L2/CU
- Req Q
- SC Q
- RetQs
- Vertical MT
- Single Thread
- SMT/ thread agnostic
POWER EFFICIENCY AND APM

- Start with inherently power-efficient micro-architecture and implementation:
  - Dynamic sharing of shared resources
  - Minimize data movement
  - Extensive clock and power gating

- Add active management support:
  - Digitally measure activity to estimate power
  - Hardware uses higher frequency when power limit allows

- Support for chip-level core power gating

Power consumption varies greatly by workload

* Based on internal AMD modeling using benchmark simulations
BUILDING A "BULLDOZER" PROCESSOR

Each processor die is composed of multiple “Bulldozer” modules. Module divisions are transparent to shared hardware, operating system or application. The modular architecture speeds chip development and increases product flexibility.

Server:
“Interlagos” – 16 cores (2 dies)
“Valencia” – 8 cores (1 die)

Client:
“Zambezi” – 8 cores (1 die)
## NEW “BULLDOZER” INSTRUCTIONS

<table>
<thead>
<tr>
<th>Instruction</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>SSSE3</strong></td>
<td>Supplemental Streaming SIMD Extensions 3 (SSSE3) is a SIMD instruction set. It contains 16 discrete instructions; because each can act on 64-bit MMX or 128-bit XMM registers it represents a total of 32 instructions.</td>
</tr>
<tr>
<td><strong>SSE 4.1</strong></td>
<td>A set of 47 instructions that execute operations which are not specific to multimedia applications. It features a number of instructions whose action is determined by a constant field and a set of instructions that take XMM0 as an implicit third operand.</td>
</tr>
<tr>
<td><strong>SSE 4.2</strong></td>
<td>An additional 7 instructions that are incremental to SSE 4.1, including 4 very powerful and generic string compare operations.</td>
</tr>
<tr>
<td><strong>AES and PCMULQDQ</strong></td>
<td>Advanced Encryption Standard (AES) Instruction Set is an extension to the x86 instruction set architecture. It helps improve the speed of applications performing encryption and decryption using the Advanced Encryption Standard (AES).</td>
</tr>
<tr>
<td><strong>AVX</strong></td>
<td>The size of the SIMD vector registers is increased from 128-bits XMM registers to 256-bits registers called YMM0 - YMM15. Existing 128-bit instructions use the lower half of the YMM registers. The AVX instruction set allows all two-operand XMM instructions to be modified into non-destructive three-operand forms where the destination register is different from both source registers.</td>
</tr>
<tr>
<td><strong>FMA4</strong></td>
<td>The FMA instruction set is a extension to the 128-bit and 256-bit SIMD instructions in the X86 microprocessor instruction set to perform fused multiply-add operations.</td>
</tr>
<tr>
<td><strong>XOP</strong></td>
<td>XOP makes the binary coding of new instructions more compatible with Intel's AVX instruction extensions, while the functionality of the instructions is unchanged.</td>
</tr>
</tbody>
</table>
“BULLDOZER”: FLEX FP OPERATING MODES

<table>
<thead>
<tr>
<th></th>
<th>Legacy</th>
<th>Core 1 AVX</th>
<th>Core 2 AVX</th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>Mode</strong></td>
<td>Legacy</td>
<td>AVX</td>
<td>AVX</td>
</tr>
<tr>
<td>Core 1 single precision</td>
<td>4</td>
<td>8</td>
<td>0</td>
</tr>
<tr>
<td>Core 1 double precision</td>
<td>2</td>
<td>4</td>
<td>0</td>
</tr>
<tr>
<td>Core 2 single precision</td>
<td>4</td>
<td>0</td>
<td>8</td>
</tr>
<tr>
<td>Core 2 double precision</td>
<td>2</td>
<td>0</td>
<td>4</td>
</tr>
<tr>
<td>FLOPs/Cycle (16 cores)</td>
<td>64</td>
<td>64</td>
<td>64</td>
</tr>
<tr>
<td>Recompiled app?</td>
<td>No</td>
<td>Yes</td>
<td>Yes</td>
</tr>
</tbody>
</table>
## GENERATIONAL COMPARISONS

<table>
<thead>
<tr>
<th>AMD Opteron™ 4100/6100 Series Processors</th>
<th>“Valencia” / “Interlagos”</th>
</tr>
</thead>
<tbody>
<tr>
<td>Cores</td>
<td></td>
</tr>
<tr>
<td>4100: 4 or 6 core; 6100: 8 or 12 core</td>
<td>4200: 6 or 8 core; 6200: 8, 12 or 16 core</td>
</tr>
<tr>
<td>Cache (L2 per core / L3 per die)</td>
<td></td>
</tr>
<tr>
<td>512KB / 6MB</td>
<td>2MB (shared between 2 cores) / 8MB</td>
</tr>
<tr>
<td>Memory Channels and speed</td>
<td></td>
</tr>
<tr>
<td>4100: two; 6100: four; up to 1333MHz</td>
<td>4200: two; 6200: four; up to 1600MHz</td>
</tr>
<tr>
<td>Floating point capability</td>
<td></td>
</tr>
<tr>
<td>128-bit FPU per core (FADD/FMUL)</td>
<td>128-bit dedicated FMAC per core or 256-bit AVX shared between 2 cores</td>
</tr>
<tr>
<td>Integer Issues Per Cycle</td>
<td></td>
</tr>
<tr>
<td>3</td>
<td>4</td>
</tr>
<tr>
<td>Turbo CORE Technology</td>
<td></td>
</tr>
<tr>
<td>No</td>
<td>Yes (+500MHz with all cores active)</td>
</tr>
<tr>
<td>Power (ACP)</td>
<td></td>
</tr>
<tr>
<td>65W, 80W, 105W</td>
<td>TBD (planned 65W, 80W, 105W)</td>
</tr>
<tr>
<td>New Instruction Sets</td>
<td></td>
</tr>
<tr>
<td>SSD3, SSE 4.1/4.2, AVX, AES, FMA4, XOP, PCLMULQDQ</td>
<td>AMD CoolCore™, C1E, C6</td>
</tr>
<tr>
<td>Power Gating</td>
<td></td>
</tr>
<tr>
<td>AMD CoolCore™, C1E</td>
<td>AMD CoolCore™, C1E, C6</td>
</tr>
<tr>
<td>Process / Die Size</td>
<td></td>
</tr>
<tr>
<td>45nm SOI</td>
<td>32nm SOI (smaller overall die size)</td>
</tr>
<tr>
<td>Performance</td>
<td></td>
</tr>
<tr>
<td>Expected up to 50% higher throughput</td>
<td></td>
</tr>
</tbody>
</table>

The above reflect current expectations regarding features and performance and is subject to change
**AMD AND GPU COMPUTING: PIONEERING INNOVATION**

- **First Development Platform**
  - Stream Computing Development Platform
  - CTM SDK

- **First with Double Precision**
  - Industry’s first double precision GPU: AMD FireStream™ 9170
  - ATI Stream SDK

- **First to 1 TFLOPS, First OpenCL CPU**
  - First to 1 TFLOPS
  - First single slot: AMD FireStream 9250
  - Industry Standard API: OpenCL announced

- **First on Top 500’s Top Ten**
  - Tianhe-1 Top500 #5
  - FireStream 9350

- **Second Generation Single Slot**
  - FireStream 9370

Timeline:
- 2006
- 2007
- 2008
- 2009
- 2010
AMD FIRESTREAM™ GPU ACCELERATORS
SOLUTIONS OPTIMIZED FOR PERFORMANCE, POWER AND DENSITY

Maximum Performance
- Fastest memory technology
- Large memory

AMD FireStream 9370
- 2.64 TFLOPS
- 528 GFLOPS DPFP
- 4GB GDDR5
- <225W
- Passive heat sink

Deployable Performance
- Highest performance per watt and density
- Low power
- Low profile
- Optimal price/performance

AMD FireStream 9350
- 2.0 TFLOPS
- 400 GFLOPS DPFP
- 2GB GDDR5
- Single slot, <150W
- Passive heat sink
ATI RADEON™ HD 5870 ("CYPRESS")

- 1600 Stream Processors
- 20 SIMD engines
- 2.72 TFLOPs SP
- 544 GFLOPs DP
OPENCL™ DEVICE EXAMPLE

- ATI Radeon™ HD 5870 GPU

1 Compute Unit
Contains 16 Stream
Cores

1 Stream Core = 5
Processing Elements
AMD RADEON™ HD 6900 SERIES

- Dual graphics engines
- New VLIW4 core architecture
- More SIMD engines and texture units
- Over 5 Gbps
- 1536 Stream Processors
- 2.7 TFLOPs SP
- 683 GFLOPs DP
NEW CORE DESIGN

- VLIW4 thread processors
  - 4-way co-issue
  - All stream processing units now have equal capabilities (no more “T-unit”)  
  - Special functions (transcendentals) occupy 3 of 4 issue slots
- Allow better utilization than previous VLIW5 design
  - Similar performance with ~10% area reduction
  - Simplified scheduling and register management
  - Extensive logic re-use
GPU COMPUTE ENHANCEMENTS

- Asynchronous dispatch
  - Execute multiple compute kernels simultaneously
  - Each kernel has its own command queue and protected virtual address domain

- Dual bidirectional DMA engines for faster system memory reads & writes

- Coalescing of shader read ops

- Fetch direct to LDS

- Improved flow control

- Faster double precision ops (1/4 SP rate)
UPCOMING POWER CONTAINMENT FEATURE DRIVES GPU PERFORMANCE EFFICIENCY

- Clamps GPU TDP to a pre-determined level
- Integrated power control processor monitors power draw every clock cycle
  - Dynamically adjusts clocks for various blocks to enforce TDP
- No longer need to constrain clock speeds to allow for outlier applications
- User controllable via AMD OverDrive Utility

Note: See slide 34 for additional information
POWER CONTAINMENT

High peak power

Lower peak power

Power containment

Unconstrained power

Scaled power

Fast completion

Slower completion

Theoretical example only
NOW THE AMD FUSION™ ERA OF COMPUTING BEGINS

- APU: Fusion of CPU & GPU compute power within one processor
- High-bandwidth I/O
Fusion APU Based PC

- **CPU**
- **CPU**
- **System Memory**
- **North Bridge**
  - 20 GB/s
- **Fusion GPU**
  - 20 GB/s
  - PCIe 12 GB/s
- **Discrete GPU**
  - 150 GB/s
- **Graphic Memory**
ATI STREAM SDK V2.3:
OPENCL™ FOR MULTICORE X86 CPUS AND GPUS

The Power of AMD Fusion™: Developers leverage heterogeneous architecture to enable superior user experience

- **Complete OpenCL™ development platform**
- **Certified OpenCL™ 1.1 compliant by The Khronos Group**
- Write code that can scale well on multi-core CPUs and GPUs
- AMD delivers on the promise of support for OpenCL™, with both high-performance CPU and GPU technologies
- Available for download now – includes documentation, samples, profilers and developer support

GPU COMPUTE OFFLOAD – 3 PHASES

Proprietary Drivers Era

- "Hacker" programmers
- Exploit early programmable "shader cores" in the GPU
- Make your program look like "graphics" to the GPU
- CUDA, Brook+, etc

2002 - 2008

Industry Standard Drivers Era

- Expert programmers
- Good APIs for compute
- "C and C++ like"
- Multiple address spaces & explicit data movement

OpenCL™/DirectCompute Driver-based APIs

2009 - 2011

Architected Era

- Mainstream programmers
- GPU is a first class member of the platform architecture
- Full C++ support
- Single unified & coherent address space

2012 - 2020

Fusion Architecture
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